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## EVAL-L9963E-MCU evaluation board

### Introduction

The EVAL-L9963E-MCU is a hardware tool for evaluation and development and is ideal for rapid prototyping of a 48 V battery management system (BMS) or as lower stage of a distributed BMS. This board can be used to evaluate the features of the L9963E device and L9963T.

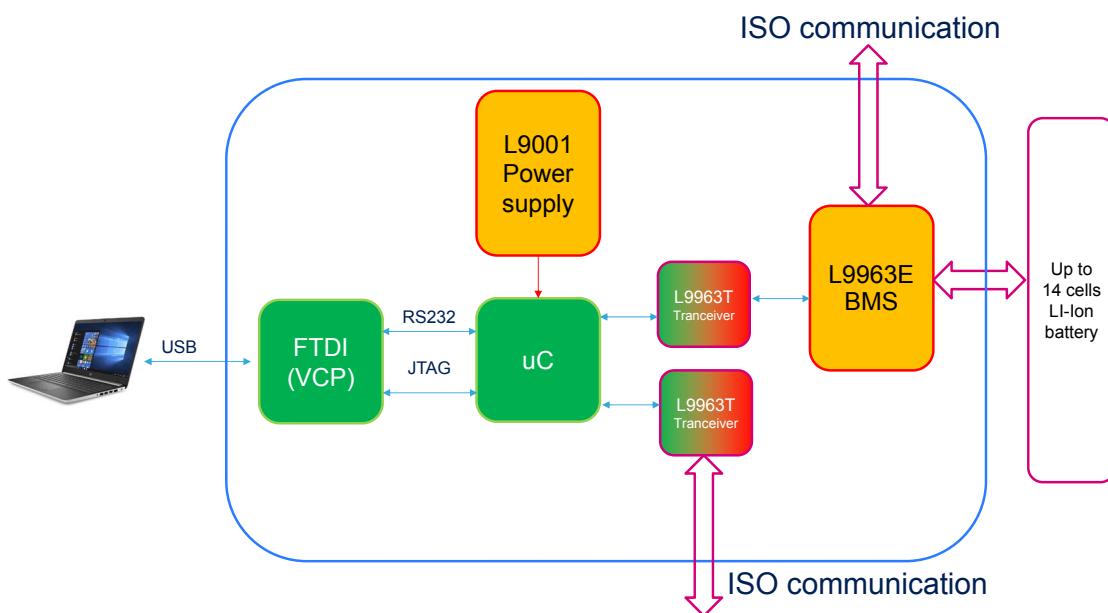
The EVAL-L9963E allows the user to connect up to 14 channels for cell voltage sensing, one channel for current sensing, and up to 4 channels for temperature sensing (plus an additional on-board NTC to sense PCB temperature). The board provides an onboard microcontroller with preloaded firmware intended to be used with STSW-L9963E GUI (graphical user interface).

## 1 Hardware description

The EVAL-L9963E-MCU board provides maximum flexibility, giving access to all pins to simplify the evaluation and debug phase of the device.

### 1.1 Block diagram

Figure 1. EVAL-L9963E-MCU block diagram



### 1.2 Featured components

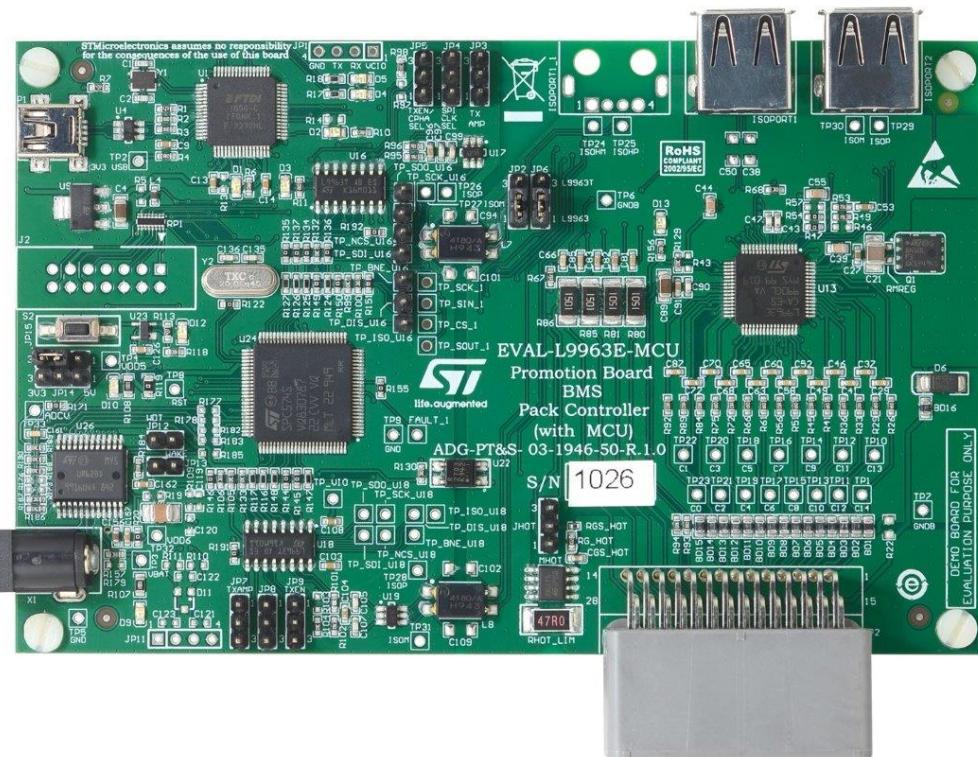
The EVAL-L9963E-MCU can be considered a reference design for a 48 V BMS or as a first layer of a distributed BMS system. In the following table there is a short description of all the ST featured components.

Table 1. Featured components

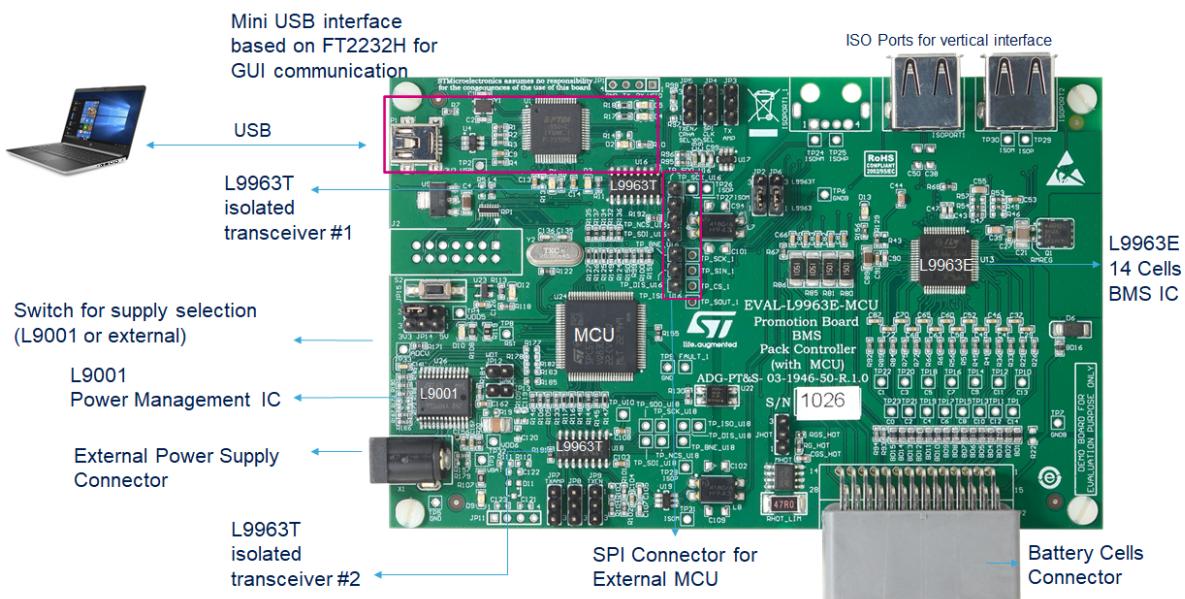
Name	Description
L9963E	Automotive chip for battery management applications
L9963T	Automotive SPI to isolated SPI transceiver
L9001	Automotive power supply IC with multiple voltage regulators
SPC574S64E3	32-bit Power Architecture MCU for automotive chassis and safety applications

## 1.3 Board description

**Figure 2. Board top view**



**Figure 3. Main components and connectors**



## 2 Jumpers and connectors

### 2.1 Mother board jumpers and connectors

Table 2. Motherboard jumpers and connectors

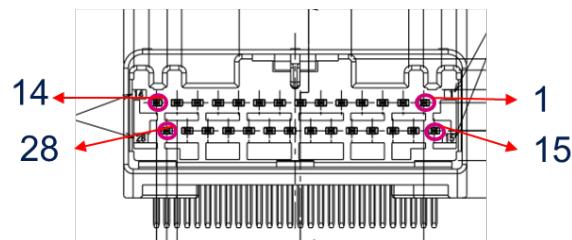
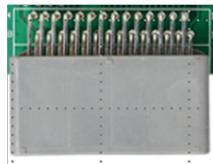
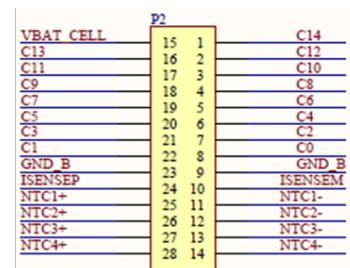
Name	Description	Type
X1	External power supply connector	Jack
P1	USB connector for PC communication	Mini USB connector
ISOPORT 1	Isolated serial communication port:	USB type A connector
	1- VBAT	
	2- ISOH- (From L9963E)	
	3- ISOH+ (From L9963E)	
	4- FaultH	
ISOPORT 2	Isolated serial communication port:	USB type A connector
	1- N.C.	
	2- ISO- (from L9963T)	
	3- ISO+ (from L9963T)	
	4- N.C.	
P2	Battery connector:	Multi pin connector
	1- cell 14	
	2- cell 12	
	3- cell 10	
	4- cell 8	
	5- cell 6	
	6- cell 4	
	7- cell 2	
	8- cell 0	
	9- ground	
	10- current sensor resistor negative pin	
	11- NTC1-	
	12- NTC2-	
	13- NTC3-	
	14- NTC4-	
	15- VBAT	
	16- cell 13	
	17- cell 11	
	18- cell 9	
	19- cell 7	
	20- cell 5	

Name	Description	Type
P2	21- cell 3	Multi pin connector
	22- cell 1	
	23- ground	
	24- current sensor resistor positive pin	
	25- NTC1+	
	26- NTC2+	
	27- NTC3+	
	28- NTC4+	
JP2	L9963T (U16) ISO- output selection	1-2 ISO- redirected to ISOPORT 1_1 2-3 ISO- redirected to L9963E
JP3	L9963T (U16) TX amplitude selection	1-2 high amplitude/high threshold <sup>(1)</sup> 2-3 low amplitude/low threshold <sup>(1)</sup> Unconnected : high amplitude/high threshold
JP4	L9963T (U16) SPI master clock selection	1-2 minimum frequency <sup>(1)</sup> 2-3 maximum frequency <sup>(1)</sup> Unconnected: minimum frequency
JP5	L9963T (U16) transmitter enable signal	1-2 enable the TX activity <sup>(1)</sup> 2-3 disable the TX activity <sup>(1)</sup> Unconnected : controlled by µc (PD9)
JP6	L9963T (U16) ISO+ output selection	1-2 ISO- redirected to ISOPORT 1_1 2-3 ISO- redirected to L9963E
JP7	L9963T (U18) TX amplitude selection	1-2 high amplitude/high threshold <sup>(1)</sup> 2-3 low amplitude/low threshold <sup>(1)</sup> Unconnected: high amplitude/high threshold
JP8	L9963T (U18) SPI master clock selection	1-2 minimum frequency <sup>(1)</sup> 2-3 maximum frequency <sup>(1)</sup> Unconnected: minimum frequency
JP9	L9963T (U18) transmitter enable signal	1-2 enable the TX activity <sup>(1)</sup> 2-3 disable the TX activity <sup>(1)</sup> Unconnected: controlled by µc (PD8)
JP12	L9001 (U26) watchdog disable <sup>(2)</sup>	Connected: watchdog disabled Unconnected: watchdog enabled
JP13	L9001 (U26) wake signal	Connected: L9001 enabled Unconnected :L9001 disabled
JP14	3.3 V - 5 V voltage selector	1-2 5 V 2-3 3.3 V
JP15	5 V selector	1-2 5 V from L9001 2-3 5 V from USB
JHot	Hot plug voltage selector	1-2 VTREF 2-3 Vreg

1. See *L9963T datasheet*.

2. See *L9001 datasheet*.

**Figure 4. P2 Battery connector**



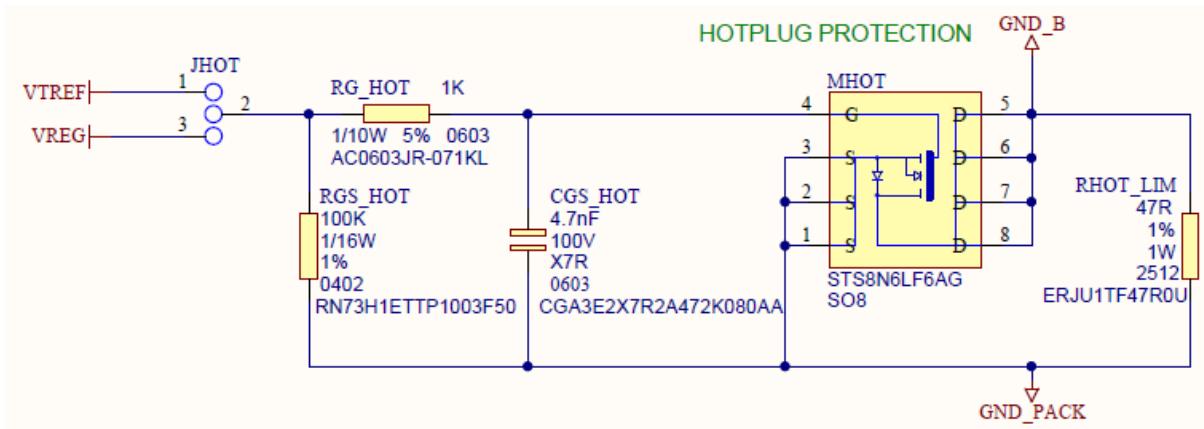
## 2.2 Default jumpers setting

**Table 3. Jumpers configuration**

Name	Description	Configuration
JP2	L9963T (U16) ISO- output selection	2-3 ISO- redirected to L9963E
JP3	L9963T (U16) TX amplitude selection	1-2: high amplitude/high threshold
JP4	L9963T (U16) SPI master clock selection	Unconnected: minimum frequency
JP5	L9963T (U16) transmitter enable signal	Unconnected: controlled by µc (PD9)
JP6	L9963T (U16) ISO+ output selection	2-3 ISO- redirected to L9963E
JP7	L9963T (U18) TX amplitude selection	1-2: high amplitude/high threshold
JP8	L9963T (U18) SPI master clock selection	Unconnected: minimum frequency
JP9	L9963T (U18) transmitter enable signal	Unconnected: controlled by µc (PD8)
JP12	L9001 (U26) watchdog disable (2)	Connected: watchdog disabled
JP13	L9001 (U26) wake signal	Connected: L9001 enabled
JP14	3.3 V - 5 V voltage selector	1-2 5 V
JP15	5 V selector	1-2 5 V from L9001
JHot	Hot plug voltage selector	1-2 VTREF

## 2.3 Hot plug protection

Figure 5. Hot plug protection circuit



The structure shown in the Figure 5 on the GND path will help withstanding the hot plug by limiting the inrush current incoming from any L9963E pin connected to the centralized clamp.

Working principle is the following:

When L9963E is OFF and no cell is connected, the VREG regulator is shut down and MHOT is safely kept off by the RPD pull down resistor.

Upon the first hot plug event, inrush current incoming from the centralized clamp is forced to flow into RHOT resistor, which offers proper limiting.

Any VDS voltage spike on MOSFET during hot plug could be coupled to the gate via the parasitic Miller capacitance. Unwanted turn-on is safely filtered by CGS, that helps keeping VGS below the threshold voltage. Hence the MOSFET will stay OFF during hot plug.

If the hot plug voltage is enough to guarantee L9963E powerup the MOSFET will be turned on by VREG regulator with a proper delay, obtained through RG gate resistor.

Finally, during L9963E normal operation the MOSFET will be ON, thus guaranteeing a very low impedance path (few mΩ) on the analog GND (GND\_B) line.

Such a small shift between L9963E GND and battery pack GND will not alter cell measurement at all, since cell ADCs are fully differential. Hence, both cell and sum of cells measurements will be accurate.

Moreover, since L9963E only drains few mA from the battery pack, error introduced on the VBAT stack measurement via internal voltage divider will be negligible.

Also the CSA used for Coulomb counting features a fully differential architecture, thus being immune to such a small common mode shift.

## 3 Getting started

### 3.1 System requirements

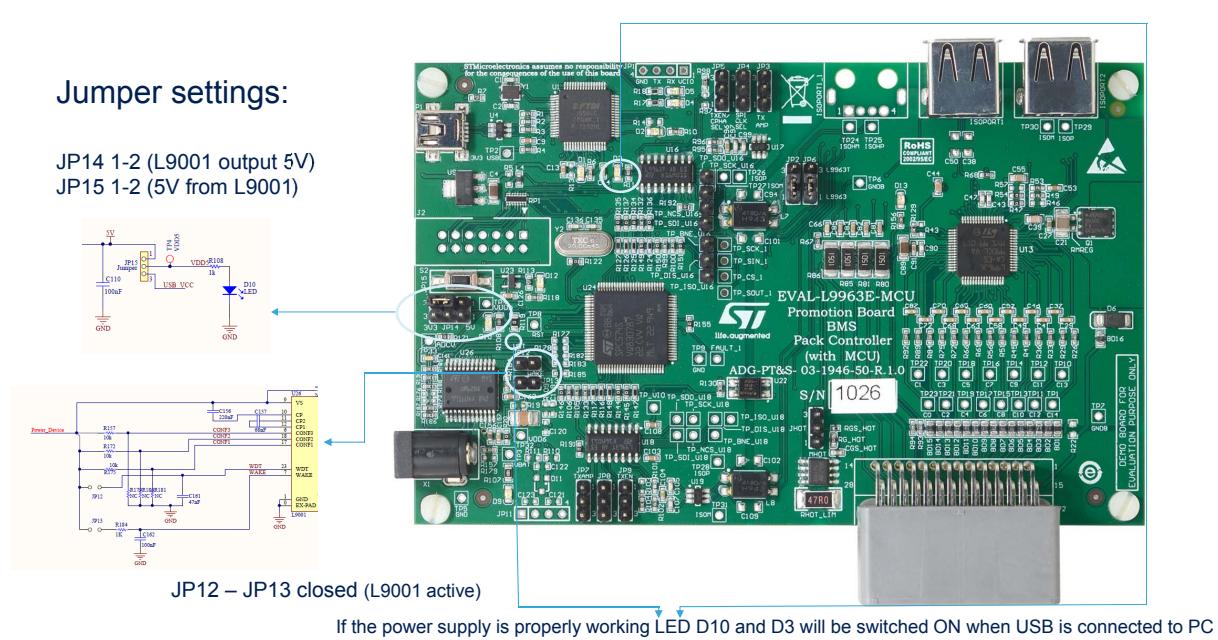
- EVAL-L9963E-MCU
- Mini USB to USB type A cable
- Power supply (at least 3 output 0 – 30 V, if possible 60 V):
  - 1 output to power L9963E (0:60 V)
  - 1 output to simulate cells common mode voltage (0:60 V)
  - 1 output to simulate cell voltage (0:5 V)
  - 12 V power supply with 2.1 mm jack output, internal pin +
- L9963E evaluation GUI (please check STSW-L9963E user manual)

### 3.2 EVAL-L9963E-MCU board setup

#### 3.2.1 Low voltage power supply

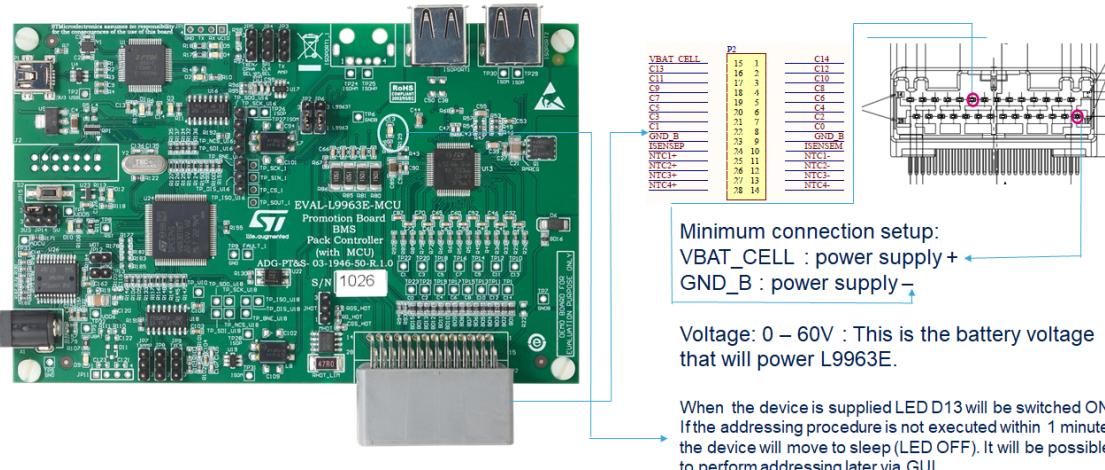
The 12 V power supply must be connected to X1 connector in order to properly supply the low voltage portion of the EVAL-L9963E-MCU board.

Figure 6. Low voltage power supply



### 3.2.2 L9963E external connection and power supply

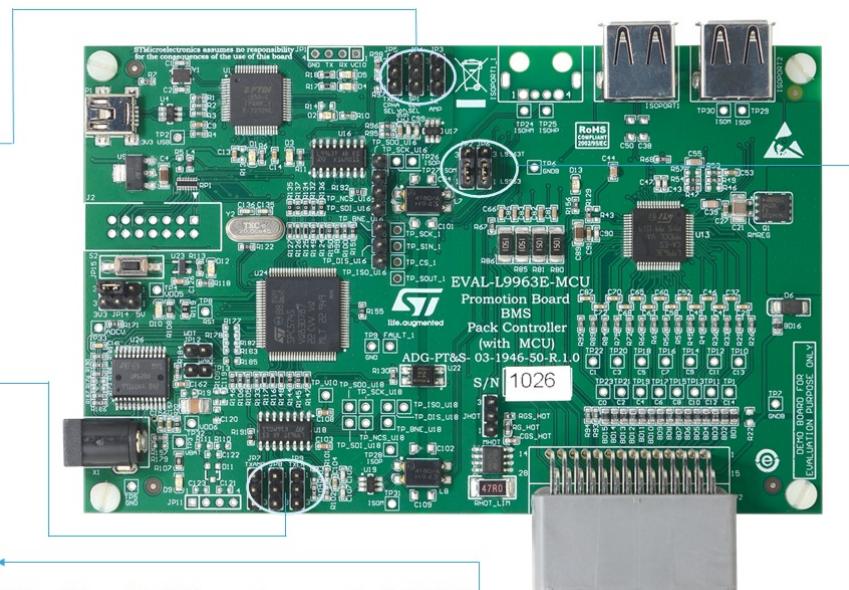
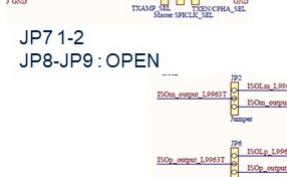
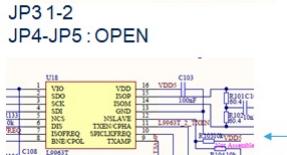
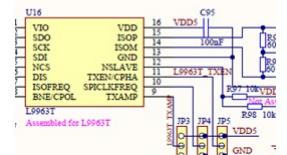
**Figure 7.** L9963E external connection and power supply



### 3.2.3 Transceiver settings

**Figure 8.** Transceiver settings

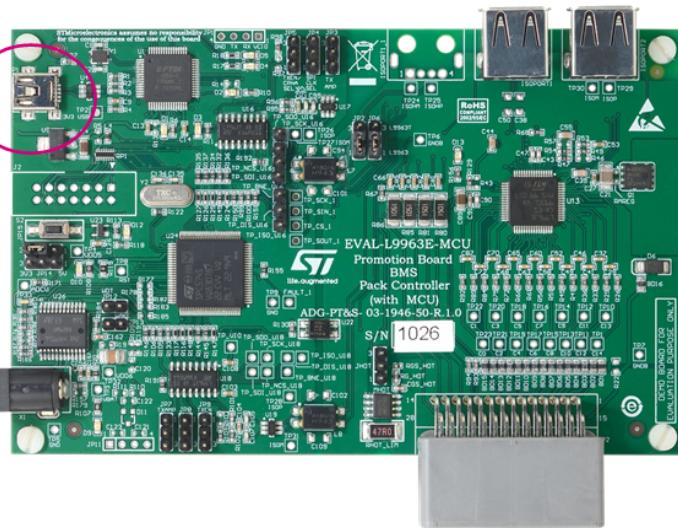
Jumper settings:



### 3.2.4 USB to PC connection

Figure 9. USB to PC connection

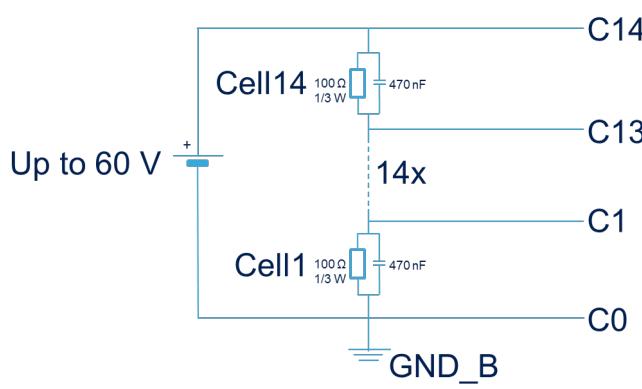
USB port to be connected to PC



### 3.2.5 Possible connection for battery simulation

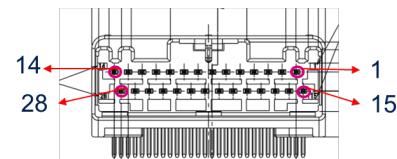
In case a real battery is not available, it's possible to use the following circuit to simulate the battery pack.

Figure 10. Battery simulation



Minimum cells set: 1,2,13,14

P2	
VBAT_CELL	
C13	15 1
C11	16 2
C9	17 3
C7	18 4
C5	19 5
C3	20 6
C1	21 7
GND_B	22 8
ISENSEP	23 9
NTC1+	24 10
NTC2+	25 11
NTC3+	26 12
NTC4+	27 13
	28 14



4

## Board schematics

**Figure 11. Board schematic (1/5)**

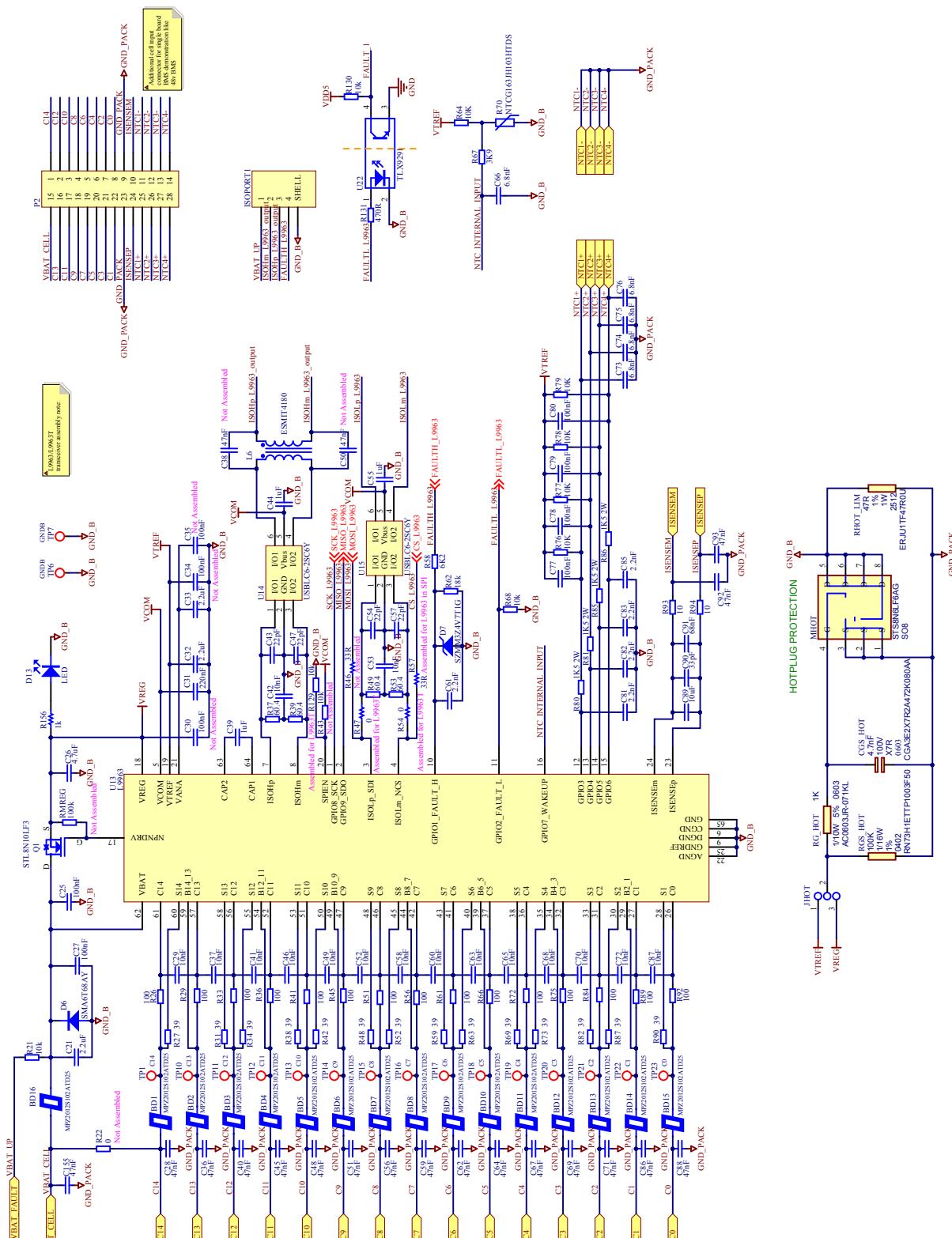
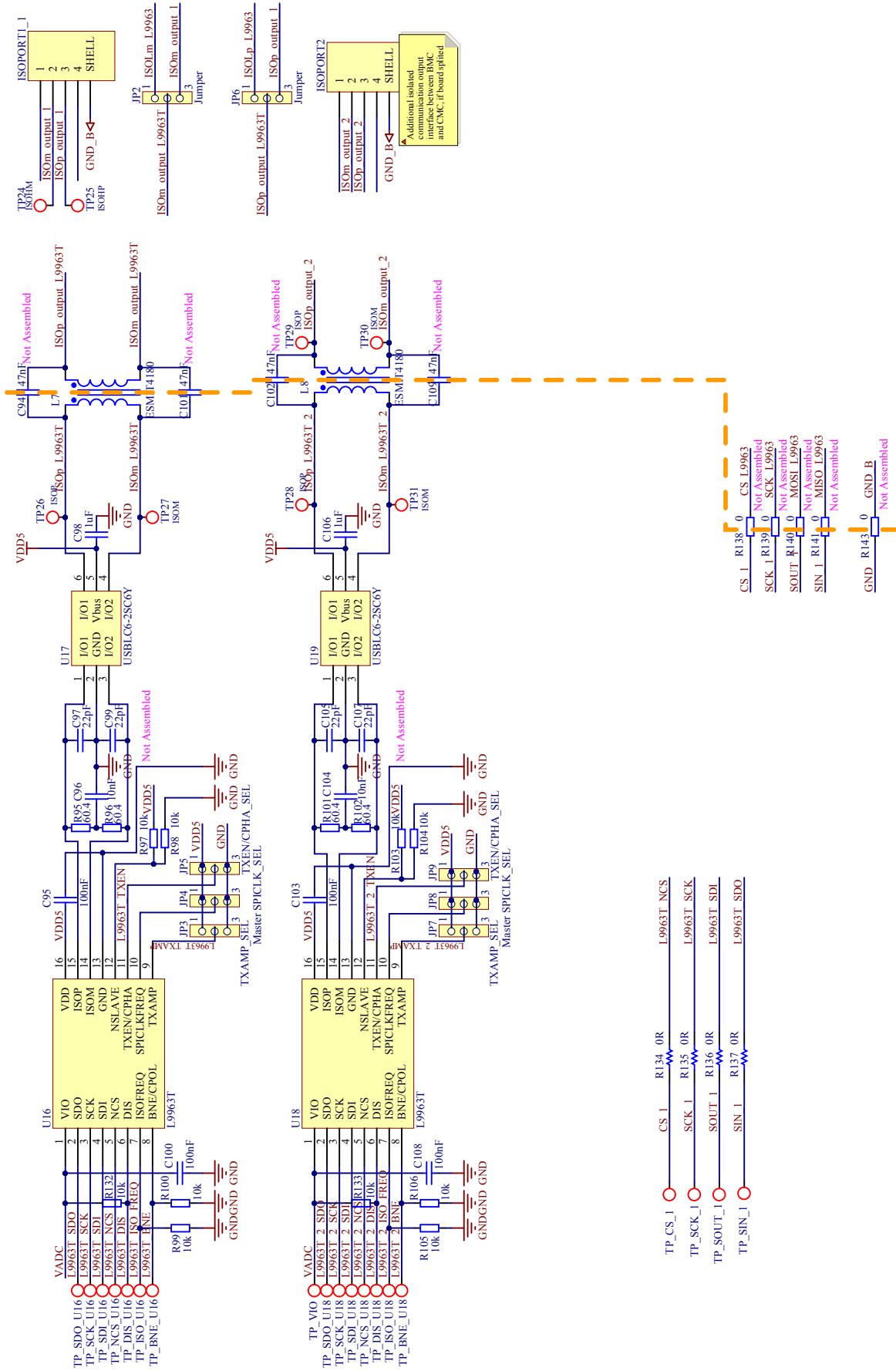
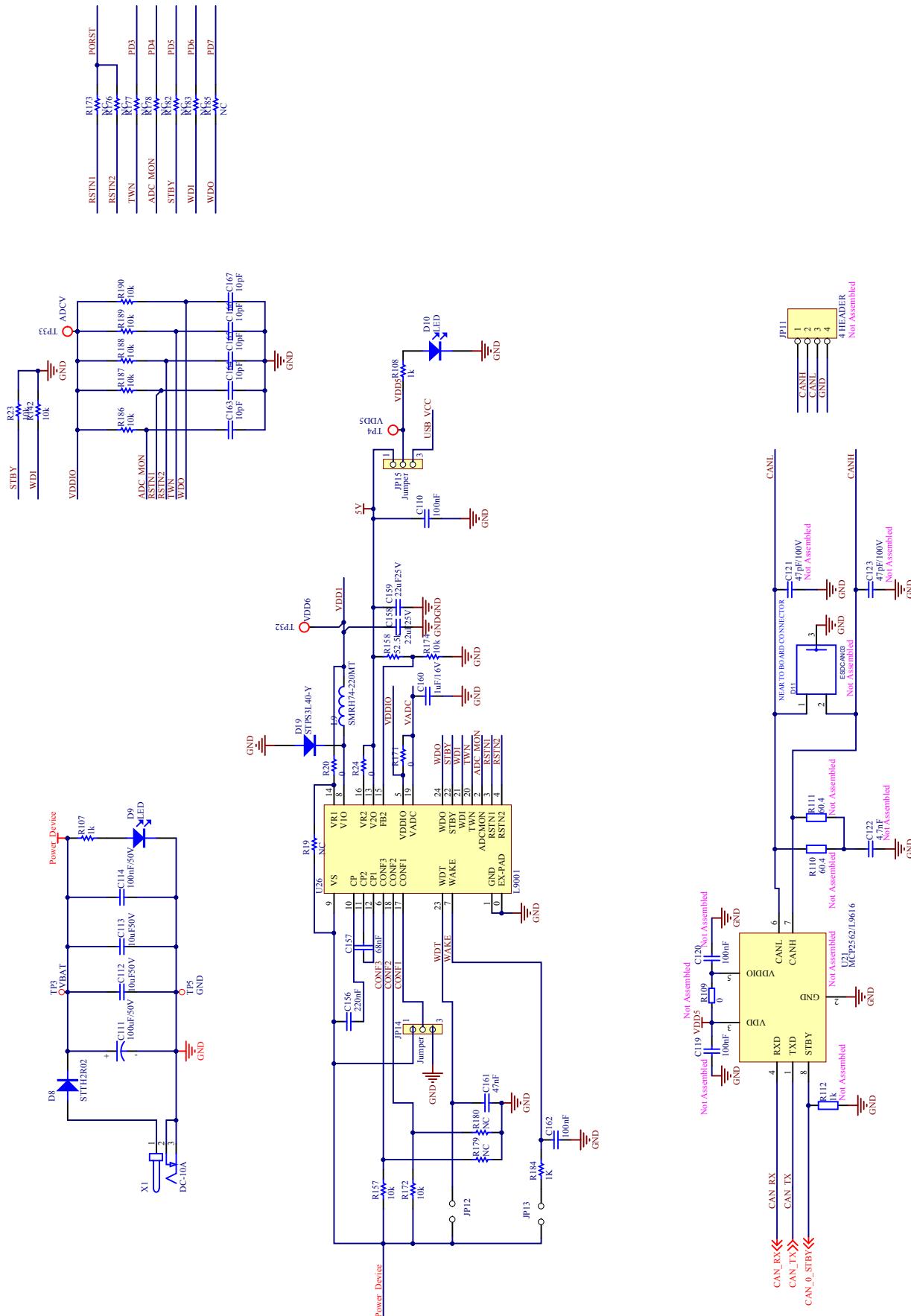


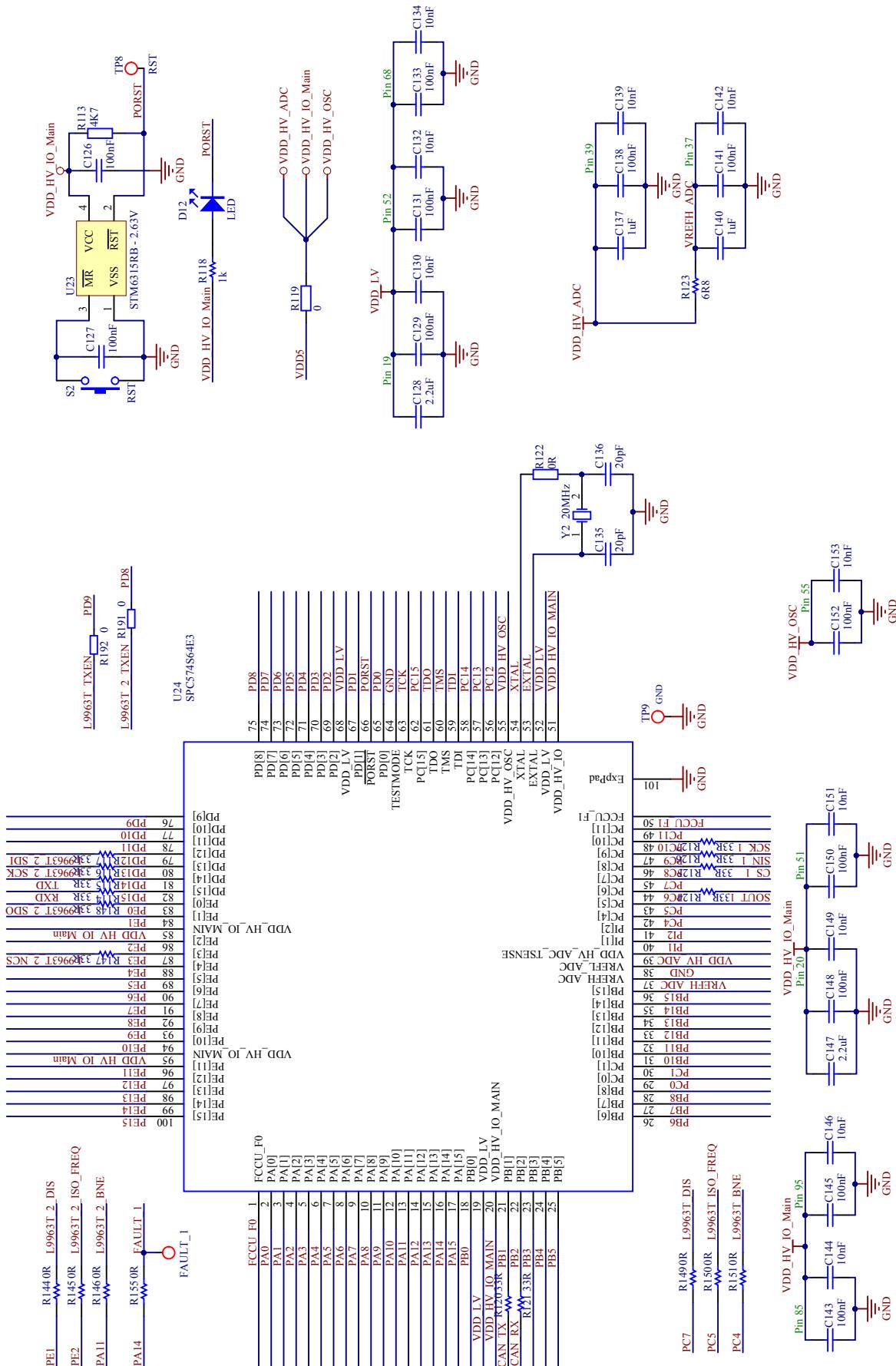
Figure 12. Board schematic (2/5)



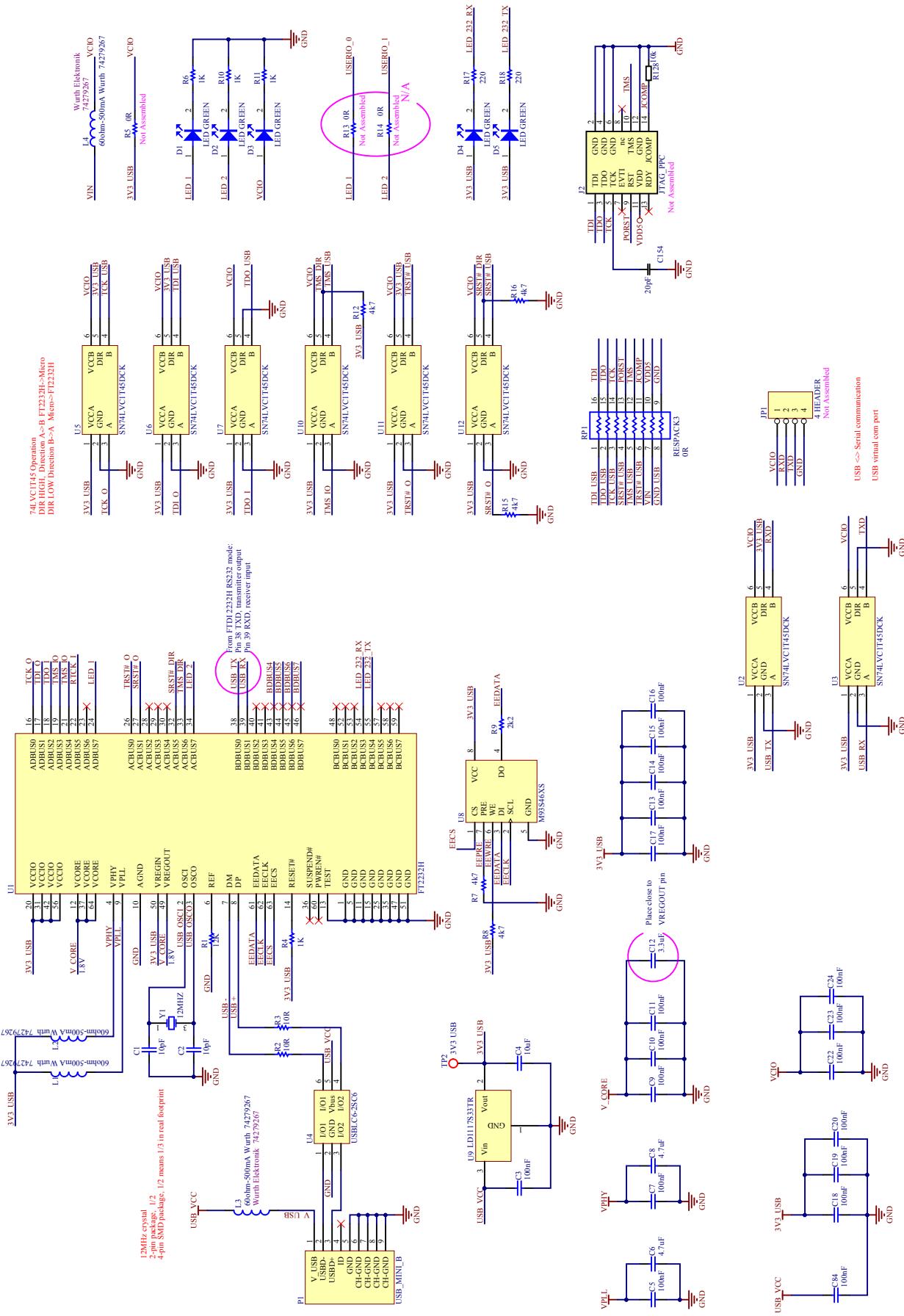
**Figure 13. Board schematic (3/5)**



**Figure 14. Board schematic (4/5)**

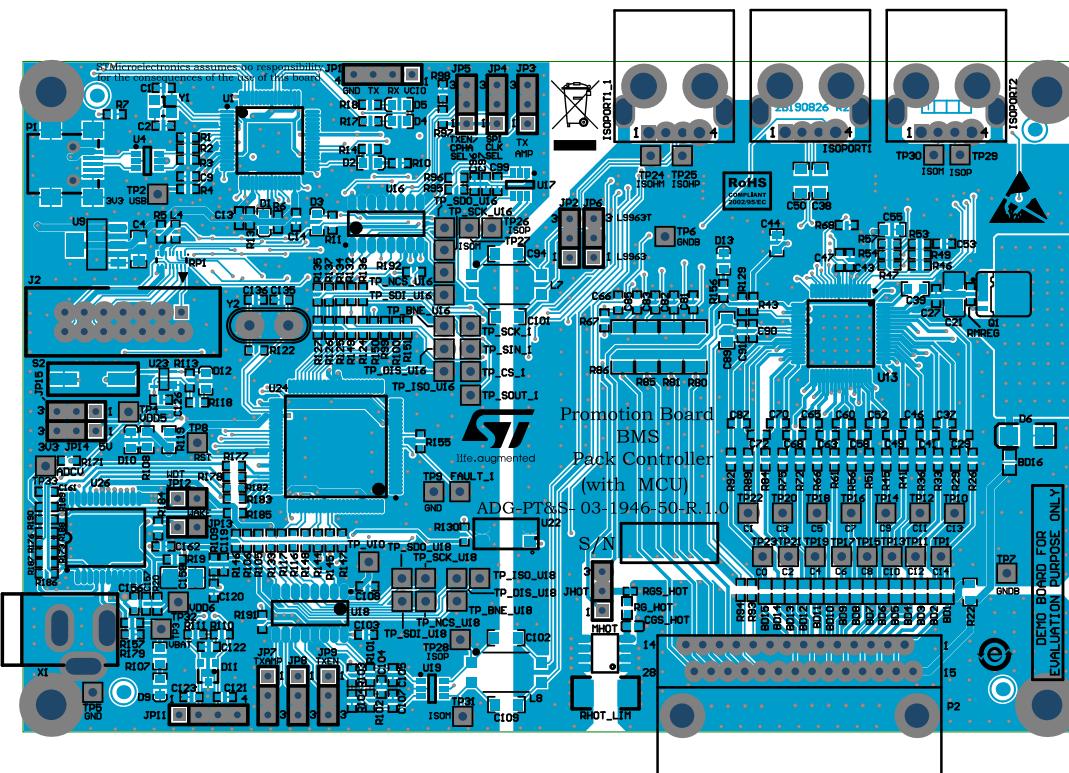


**Figure 15. Board schematic (5/5)**

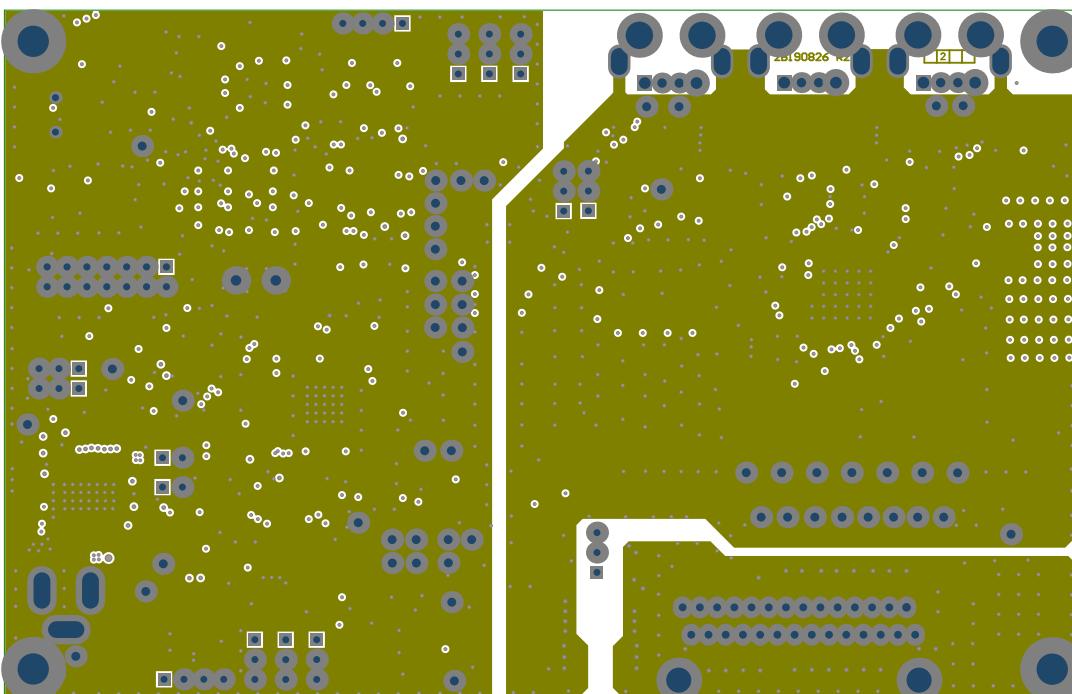


## 5 Board layout

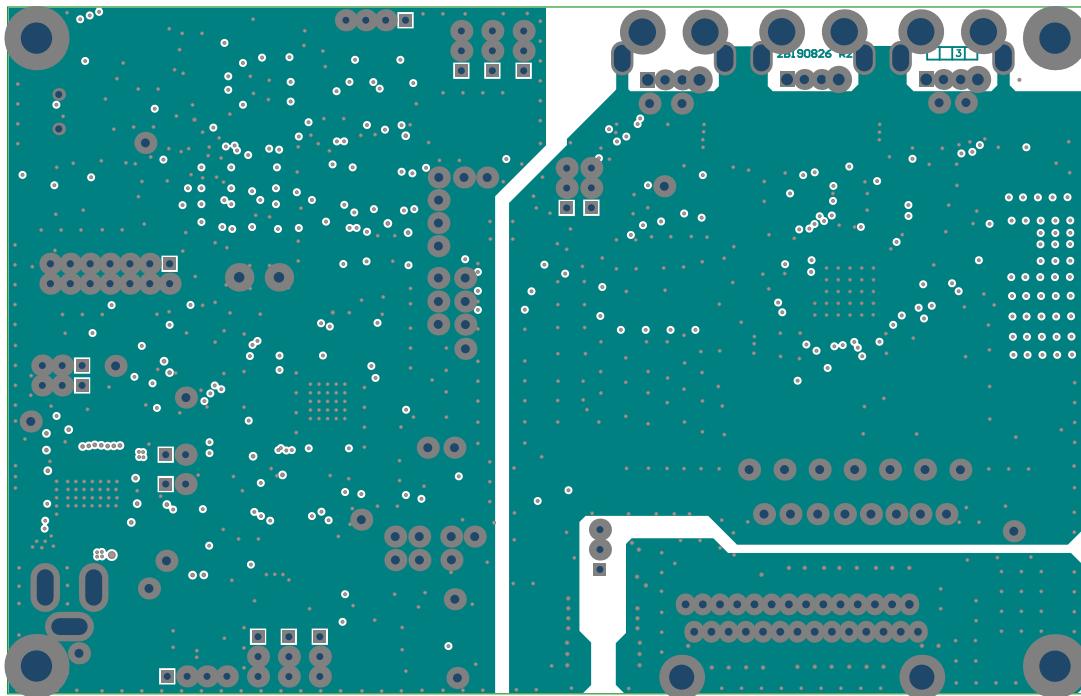
**Figure 16. Assembly top**



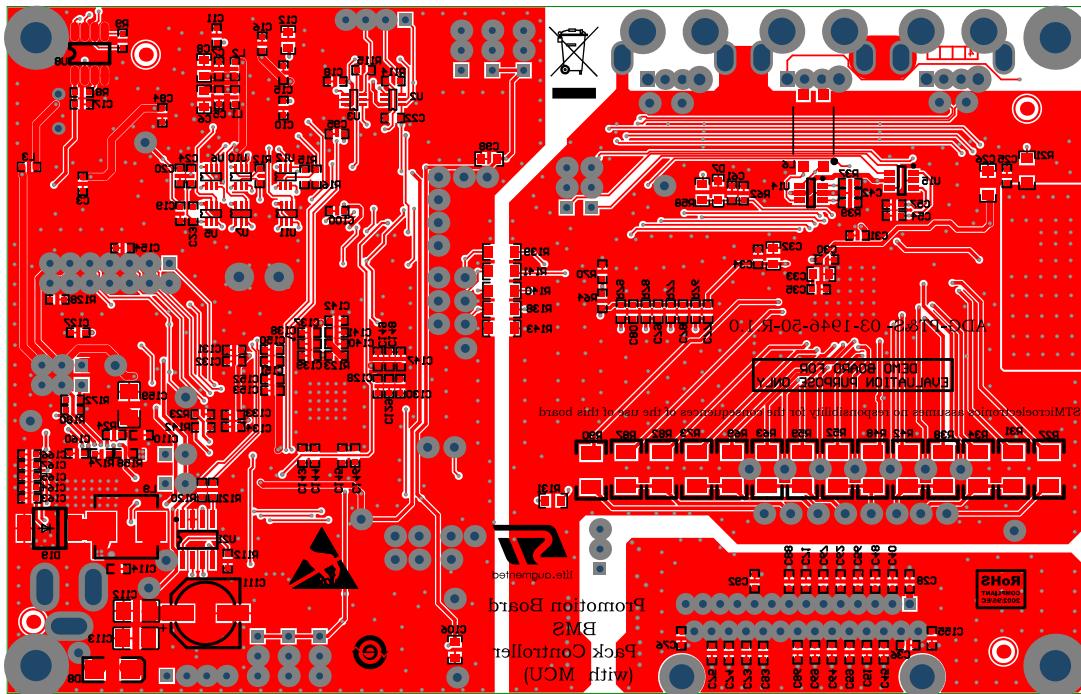
**Figure 17. Inner 1**



**Figure 18. Inner 2**

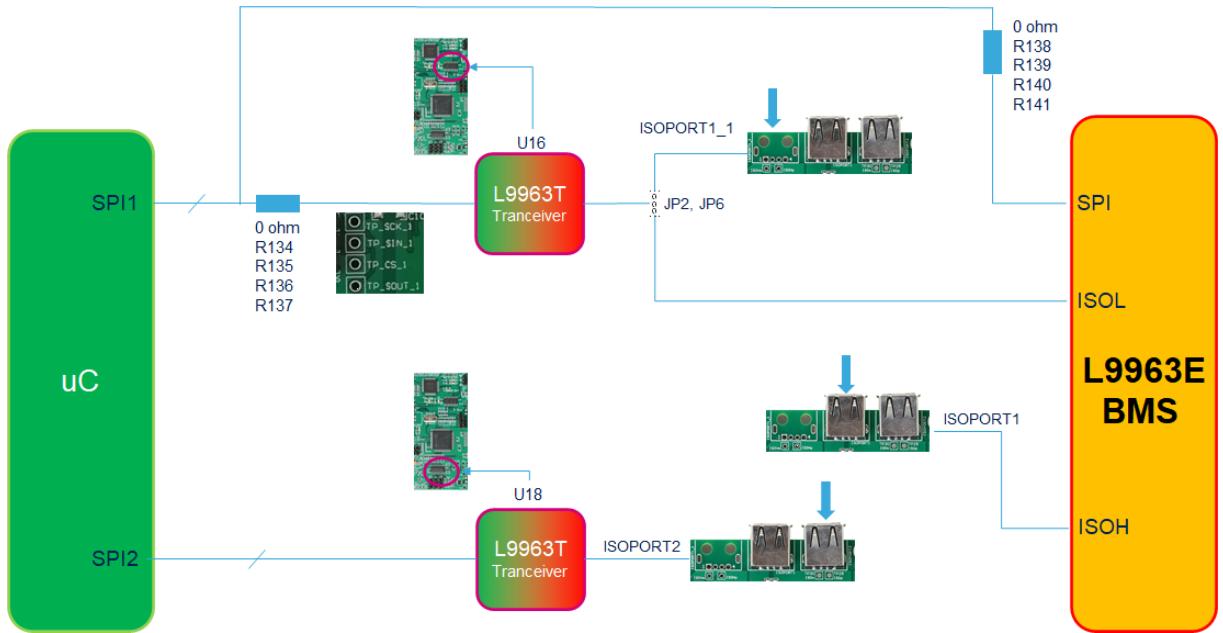


**Figure 19. Assembly bottom**



## 6 Internal and external communication configuration

Figure 20. Internal and external communication configuration



## Revision history

**Table 4. Document revision history**

Date	Version	Changes
02-Mar-2021	1	Initial release.

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